CLAIMS

What is claimed is:

1. A tester for testing dice on a wafer, said tester comprising:

a wafer probe card having connections for at least one die on a wafer, wherein the connections of the wafer probe card present an impedance selected to emulate the characteristic impedance of an end-use environment for a packaged device containing the at least one die; and

tester logic, coupled to the wafer probe card, that receives test data transfers initiated by the at least one die on the wafer via the wafer probe card.

2. The tester of Claim 1, wherein the at least one die is a logic device using Rambus Signaling Levels (RSL) to communicate to other devices, the end-use environment is a Rambus channel, and the characteristic impedance is between 20 and 60 ohms.

3. The tester of Claim 1, wherein the at least one die is a logic device using Rambus Signaling Levels (RSL) to communicate to other devices, the end-use environment is a Rambus memory module, and the characteristic impedance is approximately 28 ohms.

4. The tester of Claim 1, wherein the connections comprise microsprings on at least one of the tester interface and the at least one die.

5. The tester of Claim 1, said wafer probe card including a variable impedance network having a dynamically alterable impedance selected by the tester logic.

6. The tester of Claim 1, wherein said wafer probe card includes at least one dummy packaged device to simulate operating characteristics of the end-use environment.

7. The tester of Claim 1, wherein the tester logic includes a Rambus ASIC cell (RAC) that interfaces with the wafer probe card.

8. The tester of Claim 1, wherein the tester logic further comprises:

a timing generator that generates at least one timing signal received by the tester logic and at least one corresponding timing signal received by the at least one die on the wafer, wherein the at least one timing signal coordinates data transfer between the tester logic and the at least one die; and

one or more delay elements that selectively alter the relative phases of the at least one timing signal received by the at least one die and the at least one timing signal received by the tester logic in order to test timing sensitivity of the at least one die.

9. The tester of Claim 8, wherein the one or more delay elements delay the at least one timing signal sent to the at least one die relative to the corresponding at least one timing signal sent to the tester logic.

10. The tester of Claim 9, wherein the at least one die comprises a logic device using Rambus Signaling Levels (RSL) to communicate to other devices, and wherein the at least one timing signal received by the RSL logic die comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal.

11. The tester of Claim 10, wherein the RSL logic die outputs to the tester logic data signals and row and column signals while the one or more delay elements delay the clock-from-master positive polarity clock signal (CFM) and the clock-from-master negative polarity (CFMN) clock signal to the tester logic in order to test sensitivity of the RSL logic die to the clock-to-data timing parameter for reads by the RSL logic die.

12. The tester of Claim 8, wherein the one or more delay elements delay the at least one timing signal sent to the tester logic relative to the corresponding at least one timing signal sent to the at least one die.

13. The tester of Claim 12, wherein the at least one die comprises a RSL logic die, and wherein the at least one timing signal received from the RSL logic die comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

14. The tester of Claim 13, wherein the RSL logic receives data signals from the tester logic while the one or more delay elements delay the clock-to-master (CTM) clock signal and the clock-to-master negative (CTMN) clock signal to the tester logic in order to test sensitivity of a setup and hold output timing parameter for writes by the RSL logic die.

15. The tester of Claim 8, wherein the one ore more delay elements shift the phase of the at least one timing signal received by the at least one die in small increments relative to the at least one timing signal received by the tester logic to vary the timing between reads by the at least one die and writes by the at least one die to test for worst case failures.

16. The tester of Claim 15, wherein:

the at least one die comprises a RSL logic die;

the at least one timing signal received by the RSL logic die comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal; and

the at least one timing signal received by the tester logic comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

17. A tester for testing packaged integrated circuit devices, said tester comprising:

a test fixture having connections for at least one packaged integrated circuit device, wherein the connections of the test fixture present an impedance selected to emulate the characteristic impedance of an end-use environment for the at least one packaged integrated circuit device; and

tester logic, coupled to the test fixture, that receives test data transfers initiated by the at least one packaged device via the test fixture.

18. The tester of Claim 17, wherein the at least one packaged integrated circuit device is a logic device using Rambus Signaling Levels (RSL) to communicate to other devices, the end-use environment is a Rambus channel, and the characteristic impedance is between 20 and 60 ohms.

19. The tester of Claim 17, wherein the at least one packaged integrated circuit device is a RSL logic device, the end-use environment is a Rambus memory module, and the characteristic impedance is approximately 28 ohms.

20. The tester of Claim 17, wherein the connections comprise microsprings.

21. The tester of Claim 17, said test fixture including a variable impedance network having a dynamically alterable impedance selected by the tester logic.

22. The tester of Claim 17, wherein said test fixture includes at least one dummy packaged integrated circuit device to simulate operating characteristics of the end-use environment.

23. The tester of Claim 17, wherein the at least one packaged integrated circuit device comprises a packaged RSL logic device, and wherein the tester logic includes a Rambus ASIC cell (RAC) that interfaces with the test fixture.

24. The tester of Claim 17, wherein the tester logic further comprises:

a timing generator that generates at least one timing signal received by the tester logic and at least one corresponding timing signal received by the at least one packaged integrated circuit device, wherein the at least one timing signal coordinates data transfer between the tester logic and the at least one packaged integrated circuit device; and

one or more delay elements that selectively alter the relative phases of the at least one timing signal received by the at least one packaged integrated circuit device and the at

least one timing signal received by the tester logic in order to test timing sensitivity of the at least one packaged integrated circuit device.

25. The tester of Claim 24, wherein the one or more delay elements delay the at least one timing signal sent to the at least one packaged integrated circuit device relative to the corresponding at least one clock signal sent to the tester logic.

26. The tester of Claim 25, wherein the at least one packaged integrated circuit device comprises a packaged RSL logic device, and wherein the at least one timing signal received by the packaged RSL logic device comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal.

27. The tester of Claim 26, wherein the packaged RSL logic device outputs to the tester logic data signals and row and column signals while the one or more delay elements delay the clock-to-master positive polarity (CTM) clock signal and the clock-to-master negative polarity (CTMN) clock signal to the packaged RSL logic device in order to test sensitivity of the packaged RSL logic device to a clock-to-data output timing parameter for reads by the packaged RSL logic device.

28. The tester of Claim 24, wherein the one or more delay elements delay the at least one timing signal sent to the tester logic relative to the corresponding at least one timing signal sent to the at least one packaged integrated circuit device.

29. The tester of Claim 28, wherein the at least one packaged integrated circuit device comprises a packaged RSL logic device, and wherein the at least one timing signal received by the tester logic comprises a clock-from-master positive polarity (CFM) clock signal and

a clock-from-master negative polarity (CFMN) clock signal.

30. The tester of Claim 23, wherein the packaged RSL logic device receives data signals from the tester logic while the one or more delay elements delay the clock-from-master (CFM) clock signal and the clock-from-master negative (CFMN) clock signal to the tester logic in order to test sensitivity of setup and hold timing parameters for writes by the packaged RSL logic device.

31. The tester of Claim 25, wherein the one or more delay elements shift the phase of the at least one timing signal received by the at least one packaged integrated circuit device in small increments relative to the at least one timing signal received by the tester logic to vary the timing between reads by the at least one packaged integrated circuit device and writes by the at least one packaged integrated circuit device to test for worst case failures.

32. The tester of Claim 31, wherein:

the at least one packaged integrated circuit device comprises a packaged RSL logic device;

the at least one timing signal received by the packaged RSL logic device comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal; and

the at least one timing signal received by the tester logic comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

33. A logic tester, comprising:

a connector having connections for a logic device under test (DUT) that is one of a packaged integrated circuit device and a logic die on a wafer, wherein the connections of the connector present an impedance selected to emulate the characteristic impedance of an end-use environment for the logic DUT; and

tester logic, coupled to the apparatus, that communicates test data with the memory.

34. The logic tester of Claim 33, wherein the logic is one of a packaged logic device and a RSL logic die using Rambus Signaling Levels (RSL) to communicate to other devices, and wherein the characteristic impedance is equivalent to that of a Rambus channel or a Rambus memory module.

35. A method of testing an integrated circuit device, said method comprising:

connecting a device under test that is one of a packaged integrated circuit device and a logic die on a wafer to connections of a connector, wherein the connections present an impedance selected to emulate the characteristic impedance of an end-use environment for a packaged integrated circuit device including the device under test; and

coupling test logic to the connector; and

communicating test data transfers initiated by the device under test to the test logic via the connector to test the device under test.

36. The method of Claim 35, wherein the end-use environment is a Rambus channel and the characteristic impedance is between 20 and 60 ohms.

37. The method of Claim 35, wherein the end-use environment is a Rambus memory module and the characteristic impedance is approximately 28 ohms.

38. The method of Claim 35, wherein said connector includes a variable impedance network, and wherein communicating test data between the device under test and the test logic comprises communicating test data with said variable impedance network set to multiple different impedances.

39. The method of Claim 35, and further comprising interfacing the connector to the tester logic with a Rambus ASIC cell (RAC).

40. The method of Claim 35, and further comprising:

generating at least one first timing signal received by the tester logic and at least one second timing signal received by the device under test, wherein the first and second timing signals coordinate data transfer between the tester logic and the device under test; and

selectively altering the phase of one of the first timing signal and the second timing signal to test timing sensitivity of the device under test.

41. The method of Claim 40, wherein selectively altering comprises delaying the second timing signal sent to the device under test.

42. The method of Claim 40, wherein the device under test uses Rambus Level (RSL) to communicate to other devices, and wherein generating at least one second timing signal comprises generating a clock-to-master (CTM) clock signal and a clock-to-master negative

(CTMN) clock signal.

43. The method of Claim 40, wherein the device under test receives data signals from the tester logic while the clock-to-master (CTM) clock signal and the clock-to-master negative (CTMN) clock signal are delayed to test sensitivity of a clock-to-data output timing parameter for reads.

44. The method of Claim 40, wherein selectively altering comprises delaying the first timing signal sent to the tester logic.

45. The method of Claim 43, wherein the at least one die uses Rambus Signaling Levels (RSL) to communicate to other devices, and wherein the first timing signal comprises a clock-from-master (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

46. The method of Claim 44, wherein the device under test outputs, to the tester logic, data signals and row and column signals while the clock-from-master (CFM) clock signal and the clock-from-master negative (CFMN) clock signal are delayed in order to test sensitivity of the device under test to the setup and hold timing parameters for writes.

47. The method of Claim 40, wherein selectively altering comprises shifting the phase of the at least one second timing signal received by the device under test in increments relative to the at least one first timing signal received by the tester logic to vary the timing between reads from the device under test and writes to the device under test to test for worst case failures.

48. A tester for testing a device under test (DUT) that is either a die on a wafer or a packaged integrated circuit device, said tester comprising:

a memory device that communicates utilizing Rambus Signaling Levels (RSL) or double data rate (DDR) communication over a synchronous dynamic memory bus; and

means for connecting said memory device to said DUT such that the DUT can perform at least one of read and write operations targeting the memory device in order to test the DUT.

49. The method of Claim 48, wherein the means for connecting said memory device to said DUT comprises one or more Rambus ASIC Cell (RAC) devices to permit the memory device to emulate a Rambus Dynamic Random Access Memory (RDRAM) device and means for connecting the RAC to the DUT.

50. The method of Claim 49, wherein the memory device and RAC together comprise a Rambus Dynamic Random Access Memory (RDRAM) device.

51. A tester for testing a device under test (DUT) that is one of a die on a wafer and a packaged integrated circuit device, said tester comprising:

a slave device capable of accepting Rambus Signaling Levels (RSL) or double data rate (DDR) transfer communications as a slave and means for connecting the slave device to said DUT such that the DUT can perform transfer operations with the slave device.

52. A tester for testing a device under test (DUT) that is one of a die on a wafer and a packaged integrated circuit device, said tester comprising:

a master device capable of initiating Rambus Signaling Levels (RSL) or double data rate (DDR) transfer communications as a master and means for connecting the master device to said DUT such that the master device can perform transfer operations with the DUT.

53. A tester for testing a device under test (DUT) that is one of a die on a wafer and a packaged integrated circuit device wherein the DUT utilizes Rambus Signaling Levels (RSL) to communicate to other devices, said tester comprising:

a memory device connected to a Rambus ASIC Cell (RAC) and means for retrieving a test vector from said memory device and transferring the test vector through said RAC as inputs to pads of the DUT such that the DUT uses the test vectors to control self-test operations.

54. The tester of Claim 53, wherein the memory device and RAC together comprise a Rambus Dynamic Random Access Memory (RDRAM) device.

55. The tester of Claim 53, and further comprising means for transferring self-test operation results from the pads of the DUT through said RAC to said memory device, such that the memory stores the self-test operation results.

56. The tester of Claim 18, wherein the at least one packaged RSL logic integrated circuit device is attached to a circuit board and the test fixture includes probes for contacting the traces of said circuit board to permit the tester logic to communicate with the at least one packaged RSL logic integrated circuit device using Rambus Signaling Levels (RSL) over a Rambus channel.

57. The tester of Claim 18, wherein the at least one packaged RSL logic integrated circuit device is attached to a circuit board and the test fixture includes a connector fitting into a socket on said circuit board to permit the tester logic to communicate with the at least one packaged RSL logic integrated circuit device using Rambus Signaling Levels (RSL) over a Rambus channel.

58. The tester of Claim 19, wherein the at least one packaged RSL logic integrated circuit device is attached to a circuit board and the test fixture includes probes for contacting traces of said circuit board to permit the tester logic to communicate with the at least one packaged RSL logic integrated circuit device using Rambus Signaling Levels (RSL) while the tester logic is emulating a Rambus memory module.

59. The tester of Claim 19, wherein the at least one packaged RSL logic integrated circuit device is attached to a circuit board and the test fixture includes a connector fitting into a socket on said circuit board to permit the tester logic to communicate with the at least one packaged RSL logic integrated circuit device using Rambus Signaling Levels (RSL) while the tester logic is emulating Rambus memory module.

60. The tester of Claim 1, wherein the at least one die comprises a logic device using a double data rate (DDR) synchronous dynamic memory bus to communicate to other devices.

61. The tester of Claim 60, wherein the end-use environment is a DDR memory module and the characteristic impedance is approximately 60 ohms.

62. The tester of Claim 1, wherein the tester logic includes one or more double data rate (DDR) synchronous dynamic memory devices that interface with the wafer probe card.

63. The tester of Claim 8, wherein the at least one die comprises a DDR logic die using double data rate (DDR) synchronous dynamic memory bus to communicate to other devices, and wherein the at least one timing signal received by the DDR logic die comprises a data strobe (DQS) timing signal and the at least one corresponding timing signal received by the tester logic comprises a data strobe (DQS) timing signal.

64. The tester of Claim 63, and further comprising one or more delay elements that alter the relative timing of the DQS timing signal sent to the tester logic and the DQS timing signal sent to the DDR logic die.

65. The tester of Claim 64, wherein the DDR logic die outputs, to the tester logic, data signals while the one or more delay elements delay the data strobe (DQS) timing signal to the tester logic in order to test sensitivity of the DDR logic die to the clock-to-data timing parameter for reads by the DDR logic die.

66. The tester of Claim 64, wherein the DDR logic receives data signals from the tester logic while the one or more delay elements delay data strobe (DQS) timing signal to the tester logic in order to test sensitivity of a setup and hold output timing parameter for writes by the DDR logic die.

67. The tester of Claim 66, wherein the one or more delay elements shift the phase of the DQS timing signal received by the DDR logic die in small increments relative to the DQS timing signal received by the tester logic to vary the timing between reads by the DDR logic die and writes by the DDR logic die to test for worst case failures.

68. The tester of Claim 1, wherein the tester logic includes at least one double data rate (DDR) synchronous dynamic memory module that interfaces with the wafer probe card.

69. The tester of Claim 17, wherein the at least one packaged integrated circuit device comprises a DDR logic device that uses a double data rate (DDR) synchronous dynamic memory bus to communicate to other devices, the end-use environment is a DDR memory module, and the characteristic impedance is approximately 60 ohms.

70. The tester of Claim 17, wherein the at least one packaged integrated circuit device comprises a packaged DDR logic device, and wherein the tester logic includes one or more double data rate (DDR) synchronous dynamic memory devices that interface with the test fixture.

71. The tester of Claim 24, wherein the at least one packaged integrated circuit device comprises a packaged DDR logic device, and wherein the at least one timing signal received by the packaged DDR logic device comprises a data strobe (DQS) timing signal and wherein the at least one corresponding timing signal received by the tester logic comprises a data strobe (DQS) timing signal.

72. The tester of Claim 71, wherein the packaged DDR logic device outputs to the tester logic data signals while the one or more delay elements delay the data strobe (DQS) timing signal to the packaged DDR logic device in order to test sensitivity of the packaged DDR logic device to a clock-to-data output timing parameter for reads by the packaged RSL logic device.

73. The tester of Claim 71, wherein the packaged DDR logic device receives data signals from the tester logic while the one or more delay elements delay the data strobe (DQS) timing signal to the tester logic to test setup and hold timing parameters for writes by the packaged DDR logic device.

74. The tester of Claim 73, wherein the one or more delay elements shift the phase of the DQS timing signal received by the at least one packaged integrated circuit device in small increments relative to the DQS timing signal received by the tester logic to vary the timing between reads by the at least one packaged integrated circuit device and writes by the at least one packaged integrated circuit device to test for worst case failures.

75. The method of Claim 35, wherein the at least one die comprises a DDR logic device that employs a double data rate (DDR) synchronous dynamic memory bus to communicate to other devices, the end-use environment is a DDR memory module, and the characteristic impedance is approximately 60 ohms.

76. The method of Claim 35, and further comprising interfacing the connector to the tester logic with one or more double data rate (DDR) synchronous dynamic memory devices.

77. The method of Claim 40, wherein the device under test uses a double data rate (DDR) synchronous dynamic memory bus to communicate to other devices, and wherein generating at least one first and at least one second timing signal comprises generating at least a first data strobe (DQS) timing signal and at least a second data strobe (DQS) timing signal.

78. The method of Claim 77, wherein the device under test receives data signals from the tester logic while the second data strobe (DQS) timing signal to the device under test is delayed to test sensitivity of a clock-to-data output timing parameter for reads.

79. The method of Claim 77, wherein the device under test outputs, to the tester logic, data signals and row and column signals while the first data strobe (DQS) timing signal to the tester logic is delayed in order to test sensitivity of the device under test to the setup and hold timing parameters for writes.

80. A tester for testing a device under test (DUT) that is one of a die on a wafer and a packaged integrated circuit memory device, wherein the DUT is designed to use a double data rate (DDR) synchronous dynamic memory bus to communicate to other devices, said tester comprising:

a double data rate (DDR) synchronous dynamic memory device and means for retrieving a test vector from said DDR synchronous dynamic memory device and transferring the test vector as inputs to pads of said DUT, such that the DUT utilizes the test vectors to perform self-test operations.

81. The tester of Claim 80, and further comprising means for transferring self-test operation results from the pads of said DUT to said DDR memory device, such that the DDR memory device stores the self-test operation results.

82. The tester of Claim 69, wherein the at least one packaged DDR logic integrated circuit device is attached to a circuit board and the test fixture includes probes for contacting traces of said circuit board to permit the tester logic to communicate with the at least one packaged DDR logic integrated circuit device using a DDR synchronous dynamic memory

bus.

83. The tester of Claim 69, wherein the at least one packaged DDR logic integrated circuit device is attached to a circuit board and the test fixture includes probes for contacting traces of said circuit board to permit the tester logic to communicate with the at least one packaged logic integrated circuit device using a double data rate synchronous dynamic (DDR) memory bus while the tester logic is emulating a DDR memory module.

84. The tester of Claim 69, wherein the at least one packaged DDR logic integrated circuit device is attached to a circuit board and the test fixture includes a connector fitting into a socket on said circuit board to permit the tester logic to communicate with the at least one packaged logic integrated circuit device using double data rate (DDR) synchronous dynamic memory bus while the tester logic is emulating DDR memory module.